storage circuitry for holding a plurality of instructions at respective storage locations;

instruction fetch circuitry for fetching instructions from said storage circuitry, the instruction fetch circuitry including an indicator for providing an indication of a next address at which a next fetch operation is to be effected and a first and second instruction fetcher for fetching, respectively, a subsequent instruction and a new instruction; and

execution circuitry for executing fetched instructions comprising a branch instruction indicating a target location from which the subsequent instruction may be fetched, wherein said instruction fetch circuitry is operated responsive to execution of said branch instruction to fetch in parallel the subsequent instruction and the new instruction from said target location.

39. (New) The computer system according to claim 38, wherein the fetched instructions further comprise a condition instruction which defines a condition and determines that further instructions to be executed are new instructions only if that condition is satisfied.

40. (New) The computer system according to claim 39, wherein the fetched instructions further comprise an effect branch instruction for implementing the branch.

41. (New) The computer system according to claim 40, the system further comprising select circuitry responsive to execution of the effect branch instruction to cause said execution circuitry to execute said new instructions if the condition defined by the condition instruction is satisfied wherein said select circuitry is operable to connect a selected one of said first and second instruction fetchers to said execution circuitry.

42. (New) The computer system according to claim 40, wherein said instruction fetch circuitry comprises two instruction buffers, a first buffer for holding subsequent instructions connected to said execution circuitry, and a second buffer for holding new instructions wherein the contents of said second buffer are copied into said first buffer responsive to execution of said effect branch instruction.

43. (New) The computer system according to claim 40, wherein said instruction fetch circuitry comprises a third instruction fetcher for fetching instructions to implement predicted conditional instructions.

44. (New) The computer system according to claim 38, wherein the target location holds an address from which a first instruction of a string of new instructions is to be fetched.

45. (New) The computer system according to claim 38, wherein the branch instruction identifies a special register which holds an address from which the first instruction of a string of new instructions is to be fetched.

46. (New) The computer system according to claim 38, wherein the target location holds an address of a memory location which holds an address of a first instruction of a string of new instructions to be fetched.

47. (New) The computer system according to claim 38, further comprising decode circuitry for decoding said fetched instructions, said instruction fetch circuitry, decode circuitry and execution circuitry being arranged in pipeline.

48. (New) The computer system according to claim 40, wherein said effect branch instruction is located at a branch point after which said new instruction is to be executed.

49. (New) The computer system according to claim 38, wherein the plurality of instructions are arranged in a plurality of instruction strings, each string comprising the first instruction and the plurality of subsequent instructions.

50. (New) The computer system according to claim 49, wherein said effect branch instruction is located in the string prior to the branch point after which effect branch instructions to be executed are said new instructions, said further instruction indicating the branch point and wherein the computer system comprises a branch point register for holding said branch point.

51. (New) The computer system according to claim 38, the computer system further comprising a return register for holding a return address being the address of the next instruction

after said branch point, wherein said further instruction is effective to save said return address in said return register and wherein said set branch instruction identifies said return register to indicate the target location.

52. (New) A method of operating a computer to fetch decode and execute instructions which computer has storage circuitry holding a plurality of instructions at respective storage locations, said plurality of instructions being arranged in instructions strings, each string comprising a first instruction and a set of subsequent instructions the method comprising:

fetching instructions from said storage circuitry and providing an indication of a next address at which a next fetch operation is to be effected, wherein a first instruction fetcher fetches subsequent instructions and a second instruction fetcher fetches new instructions;

decoding said fetched instructions;

executing said fetched instructions comprising a branch instruction indicating a target location from which a subsequent instruction may be fetched, the subsequent instruction being from a different instruction string.

53. (New) The method according to claim 52, wherein said fetched instructions further comprise a condition instruction which defines a condition for a branch to be taken.

54. (New) The method according to claim 53, wherein said fetched instructions further comprise an effect branch instruction for implementing the branch;

on execution of said branch instruction, holding the indication of said target location in a target store, fetching in parallel the subsequent instructions from the string containing said branch instruction and the new instructions from said different instruction string commencing from said target location;

continuing to execute said subsequent instructions until the effect branch instruction is executed which indicates that further instructions to be executed are said new instructions if the condition defined by the condition instruction is satisfied; and

responding to said effect branch instruction by commencing execution of said new instructions, said effect branch instruction selecting which of said first and second instruction fetchers supplies instructions for execution.